Order Number: MC33883/D
Rev 3.2, 05/2001

MOTOROLA

MC33883

Advance Information

Full Bridge Pre-Driver

55 VOLTS

SEMICONDUCTOR TECHNICAL DATA

The MC33883 is a full bridge pre-driver including integrated charge pump, two independent high and low side driver channels.

The drive outputs are capable to source and sink 1 A pulse peak current. The low side channel is referenced to ground, the high side channel is floating above ground.

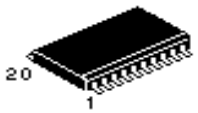
A linear regulator provides a maximum of 16.5V to supply the low side gate driver stages. The high side driver stages are supplied with a $10V_{typical}$ charge pump voltage. Such built-in feature, associated to external capacitor provides a full floating high side drive.

An under- and over-voltage protection prevents erratic system operation at abnormal supply voltages. Under fault, these functions force the driver stages into off state.

The logic inputs are compatible with standard CMOS or LSTTL outputs. The input hysteresis makes the output switching time independent of the input transition time.

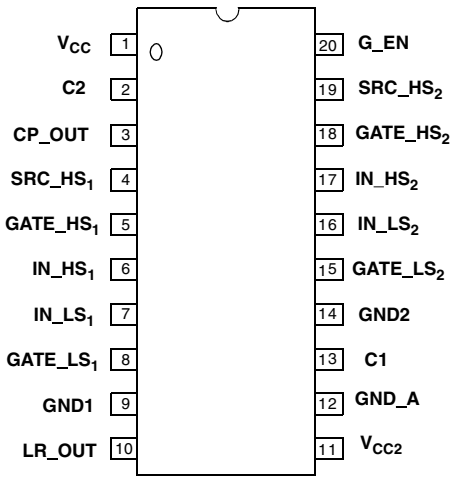
The global enable logic signal can be used to disable the charge pump and all the bias circuit. The net advantage is the reduction of the quiescent supply current to under 10µA. To wake up the circuit, 5 V has to be provided at G_EN.

- V_{CC} Operating Voltage Range from 5.5 V up to 55 V
- V_{CC2} Operating Voltage Range from 5.5 V up to 28 V
- Automotive Temperature Range -40°C to 125°C
- 1A Pulse Current Output Driver
- Fast PWM Capability
- Built-In Charge Pump



DW SUFFIX
PLASTIC PACKAGE
CASE 751D-05

PIN CONNECTIONS
(TOP VIEW)
CASE 751D-05

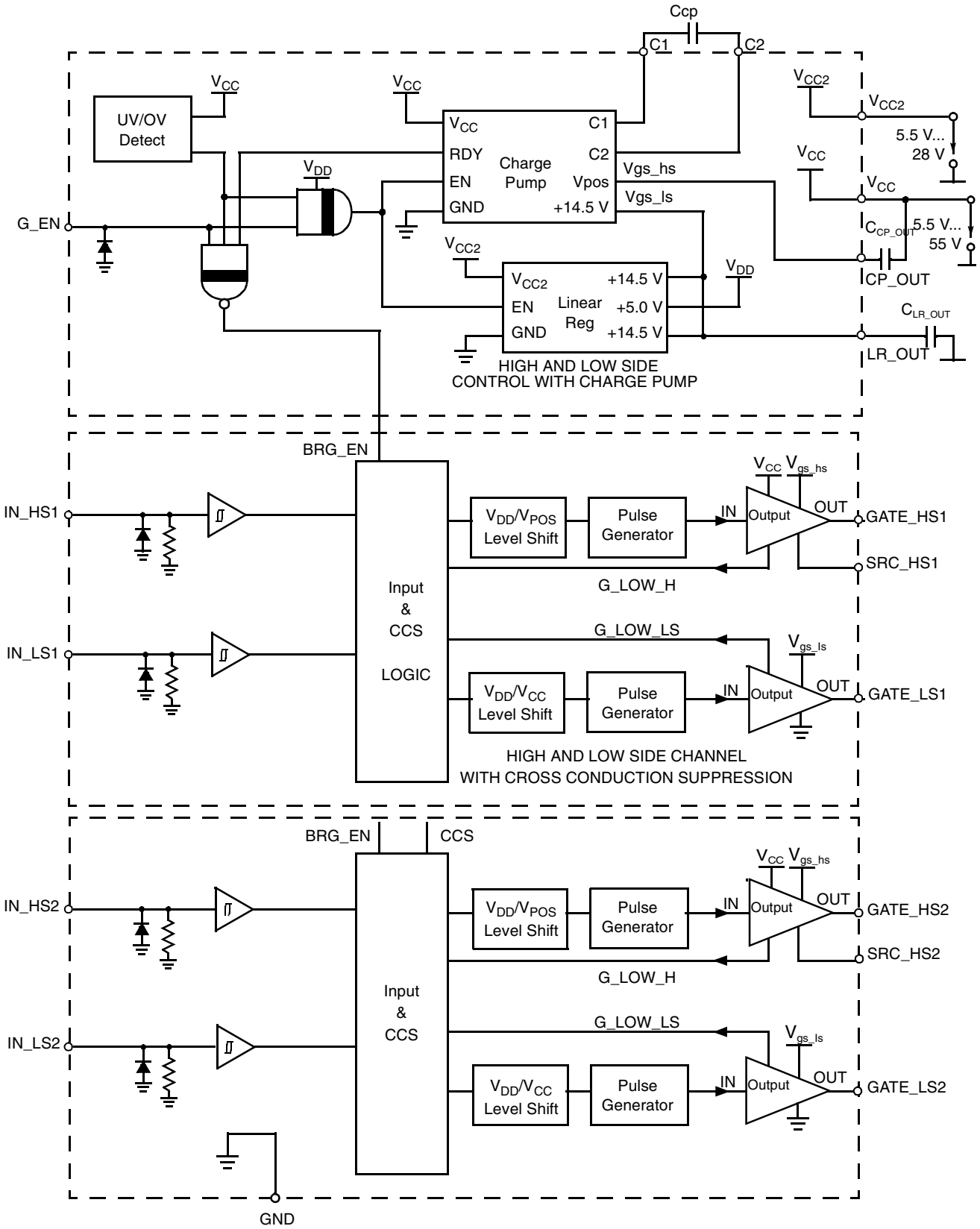


ORDERING INFORMATION		
Device	Temperature Range	Package
PC33883DW	-40°C to +125°C	SOIC20

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DEVICE DESCRIPTION

Figure 1: Principal Building Blocks



ABSOLUTE MAXIMUM RATINGS:
Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND

Rating	Symbol	Min	Max	Unit
Supply Voltage1	V_{CC}	-0.3	65	V
Supply Voltage2 (NOTE 1)	V_{CC2}	-0.3	35	V
Linear Regulator Output Voltage	V_{LR_out}	-0.3	18	V
High Side Floating Supply Absolute Voltage	V_{CP_OUT}	-0.3	65	V
High Side Floating Source Voltage	V_{SRC_HS}	-0.3	65	V
High Side Source Current from Cpout in Switch On State	I_S		250	mA
High Side Gate Voltage	V_{GATE_HS}	-0.3	65	V
High Side Gate Source Voltage	V_{GATE_HS} - V_{SRC_HS}	-0.3	20	V
High Side Floating Supply Gate Voltage	V_{CP_OUT} - V_{GATE_HS}	-0.3	65	V
Low Side Output Voltage	V_{GATE_LS}	-0.3	17	V
Wake up Voltage	V_{G_EN}	-0.3	35	V
Logic Input Voltage	V_{IN}	-0.3	10	V
Charge Pump Capacitor Voltage	V_{C1}	-0.3	V_{LR_OUT}	V
Charge Pump Capacitor Voltage	V_{C2}	-0.3	65	V
ESD Voltage on all Pins except the case of (Pin C2 respect to PinVcc) (HBM, 100pF, 1.5kOhms)	V_{ESD}	-2.0	2.0	KV
ESD Voltage (PinC2 respect to Pin Vcc)	V_{ESD2}	-1.7	1.7	KV
Power Dissipation and Thermal Characteristics				
Maximum Power Dissipation@25°C	P_D		1.25	W
Thermal Resistance Junction-to-Air	$R_{\theta JA}$		100	°C/W
Operating Junction Temperature	T_J	-40	+150	°C
Storage Temperature	T_{stg}	-65	+150	°C

OPERATING CONDITIONS:
Typical values for T_A = 25°C, Min/Max values for T_A = -40°C to +125°C

Rating	Symbol	Min	Max	Unit
Supply Voltage1	V_{CC}	5.5	55	V
Supply Voltage2	V_{CC2}	5.5	28	V
High Side Floating Supply Absolute Voltage	V_{CP_OUT}	V_{CC}+4	V_{CC}+11but<65	V

NOTE1: VCC can sustain load dump pulse 40V, 400ms, 2Ohms

STATIC ELECTRICAL CHARACTERISTICS

V_{CC} = 12 V, V_{CC2} = 12 V, C_{CP} = 33 nF, G_EN = 4.5 V unless otherwise specified.
Typical values for TA = 25°C, Min/Max values for TA = -40°C to +125°C, unless otherwise specified.

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
LOGIC SECTION						
Logic "1" Input Voltage (IN_LS & IN_HS)	6, 7, 16, 17	V_{IH}	2.0		10	V
Logic "0" Input Voltage (IN_LS & IN_HS)		V_{IL}			0.8	V
Logic "1" Input Current Vin=5V	6, 7, 16, 17	I_{in+}	200		1000	uA
Logic "0" Input Current Vin=0V		I_{in-}	200		1000	uA
Wake Up Input Voltage (G_EN)	27	V_{G_EN}	4.5	5.0	V_{CC2}	V
Wake Up Current (G_EN) V_{G_EN} = 14 V	27	I_{G_EN}		200	500	uA
Wake Up Current (G_EN) V_{G_EN} = 28V	27	I_{G_EN2}			1.5	mA
LINEAR REGULATOR SECTION						
Linear Regulator V_{LR_OUT} @ V_{CC2} from 15.0 to 28 V, I_{LOAD} from 0mA to 20mA	10	V_{LR_OUT}	12.5		16.5	V
Linear Regulator V_{LR_OUT} @ I_{LOAD} = 20mA	10	V_{LR_OUT}	V_{CC2} - 1.5			V
V_{LR_OUT} @ I_{LOAD} =20mA, V_{CC2} =5.5V, V_{CC} = 5.5V	10		4.0			V
CHARGE PUMP SECTION						
Charge Pump Output Voltage, referenced to V_{CC} V_{CC}=12V I_{LOAD} = 0mA, C_{Cpout}=1uF	3	V_{CP_OUT}	7.5			V
Charge Pump Output Voltage, referenced to V_{CC} V_{CC}=12V I_{LOAD} = 7mA, C_{Cpout}=1uF	3	V_{CP_OUT}	7.0			V
Charge Pump Output Voltage, referenced to V_{CC} V_{CC2} = V_{CC}=5.5V I_{LOAD} = 0mA, C_{Cpout}=1uF	3	V_{CP_OUT}	2.3			V
Charge Pump Output Voltage, referenced to V_{CC} V_{CC2} = V_{CC}=5.5V I_{LOAD} = 7mA, C_{Cpout}=1uF	3	V_{CP_OUT}	1.8			V
Charge Pump Output Voltage, referenced to V_{CC} V_{CC}=55V I_{LOAD} = 0mA, C_{Cpout}=1uF	3	V_{CP_OUT}	7.5			V
Charge Pump Output Voltage, referenced to V_{CC} V_{CC}=55V I_{LOAD} = 7mA, C_{Cpout}=1uF	3	V_{CP_OUT}	7.0			V
Peak current through pin C1 under rapid changing V_{cc} voltages (see Figure 5)	13	I_{C1}	-2.0		2.0	A
Minimum peak voltage at pinC1 under rapid changing V_{cc} voltages (see Figure 5)	13	V_{C1}min	-1.5			V

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE SECTION						
Quiescent Vcc Supply Current V_{G_EN}=0V @Vcc=12V	1				10	uA
Quiescent Vcc Supply Current V_{G_EN}=0V @Vcc=55V	1				10	uA
Operating Vcc Supply Current (@V_{CC}=55V and V_{CC2}=28V) (@V_{CC}=12V and V_{CC2}=12V) Logic imput pin inactive (high impedance)	 1 1			 2.2 0.7		 mA mA
Additional Operating Vcc Supply Current for EACH logic input pin active @V_{CC}=55V and V_{CC2}=28V. (Note1)	1				5	mA
Quiescent Vcc2 Supply Current V_{G_EN}=0V @ Vcc2 = 12V	11				5	uA
Quiescent Vcc2 Supply Current V_{G_EN}=0V @ Vcc2 = 28V	11				5	uA
Operating Vcc2 Supply Current (@V_{CC}=55V and V_{CC2}=28V) (@V_{CC}=12V and V_{CC2}=12V) Logic input pin inactive (high impedance)	 11 11				 10 9	 mA mA
Additional Operating Vcc2 Supply Current for EACH logic input pin active @V_{CC}=55V and V_{CC2}=28V. (Note1)	11				5	mA
Under Voltage Shutdown V_{CC2} (Note2)	11	UV2	4.0	5.0	5.5	V
Under Voltage Shutdown V_{CC}	1	UV	4.0	5.0	5.5	V
Over Voltage Shutdown V_{CC}	1	OV	57	61	65	V
Over Voltage Shutdown V_{CC2}	11	OV2	29.5	31	35	V
OUTPUT SECTION						
Output Sink Resistance (Turned off) V_{GATE_HS} - V_{SRC_HS} =1V	3, 4, 5, 8, 15, 18, 19	R_{DS}			22.0	Ohms
Output Source Resistance (Turned on) V_{CP_OUT} - V_{GATE_HS} =0.1V		R_{DS}			22.0	Ohms
High Side Source Current from CPOUT in Switch On State	4, 19	$I_S$max			200	mA
Max Voltage (V_{GATE_HS} - V_{SRC_HS}), INH=1, I_{Smax}=5mA	4, 5, 18, 19				18	V

Note 1:Large duty cycles of the logic inputs will result in a large power dissipation within the device, that possibly could surpass the package power handling rating.
Note2: Between 4.0V and 5.5V, the device can exhibt a non erroneous behaviour.

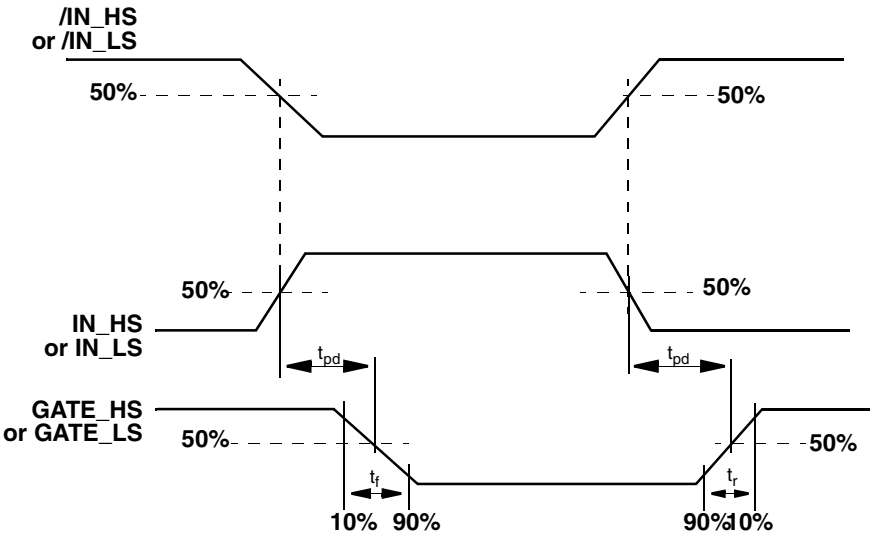
DYNAMIC ELECTRICAL CHARACTERISTICS:
V_{CC} = 12 V, V_{CC2} = 12 V, C_{CP} = 33 nF, G_EN = 4.5 V unless otherwise specified.
Typical values for TA = 25°C, Min/Max values for TA = -40°C to +125°C, unless otherwise specified

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
Prop. Delay HS and LS, C_{load}=5nF; Between 50% Input to 50% Output (see Figure 2:)	5, 6, 7, 8, 15, 16, 17, 18	t_{PD}		200	300	ns
Turn On Rise Time, C_{load}=5nF ; 10% to 90% (NOTE 3) (see Figure 2:)	5, 8, 15, 18	t_r		80	180	ns
Turn Off Fall Time, C_{load}=5nF ; 10% to 90% (NOTE 3) (seeFigure 2:)		t_f		80	180	ns

NOTE 1: Characterization only
NOTE 2: Input overdrive 1V
NOTE 3: Rise time is given by time needed to charge the gate from 1V to 10V (Vice versa for fall time)

NOTE : C_{load} corresponds to a capacitor between GATE_HS and SRC_HS for the high side and between GATE_LS and ground for low side.

Figure 2: Dynamic Characteristics



DEVICE DESCRIPTION

Driver Characteristics

Turn-On:

For turn-on the current required to charge the gate source capacitor C_{iss} in the specified time can be calculated as follows:

Peak Current for Rise/Fall Time (tr) and a typical PowerMos-FET Gate Charge Q_g

$I_P = Q_g/tr = 80nC/80\ ns \approx 1.0\ A$

Turn-Off:

The peak current for turn-off can be obtained in the same way as for turn-on. In addition to the dynamically current, required to turn-off or turn-on the FET, various application related switching scenarios have to be considered:

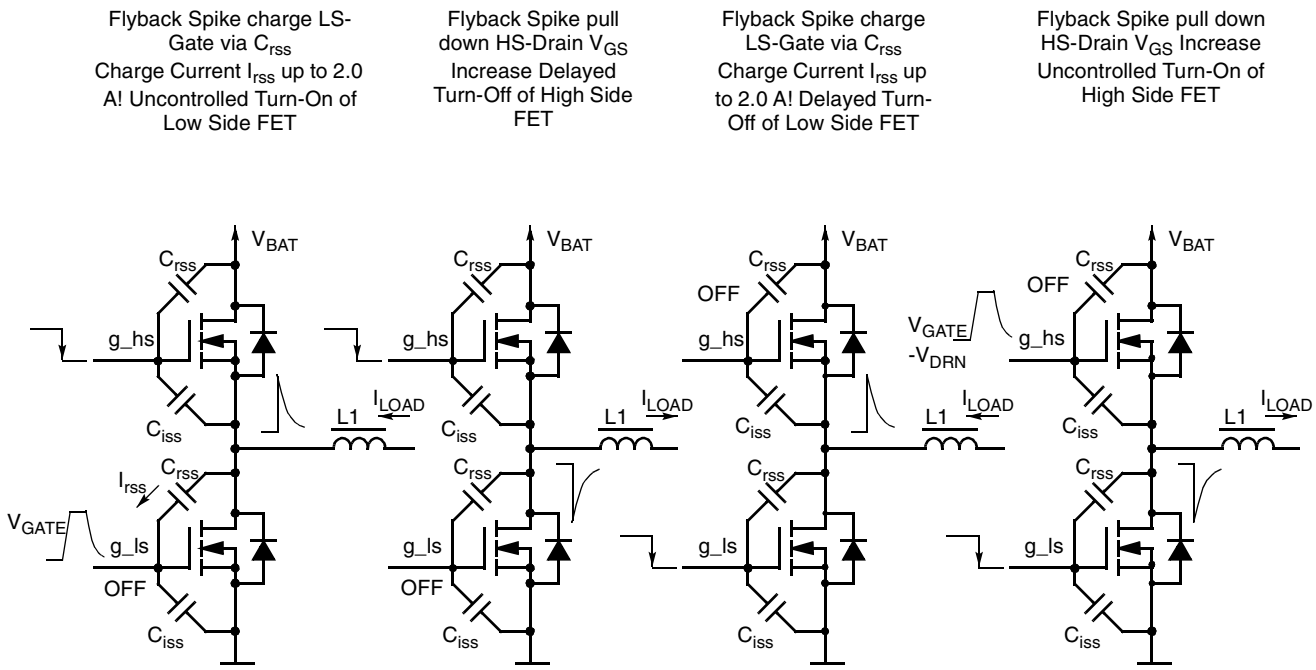
The output driver sources a peak current of up to 1A for 200ns to turn on the gate. After 200ns, 100mA is provided continuously to maintain the gate charged.

The output driver sinks a peak current of up to 1A for 200ns to turn off the gate.

After 200ns, 100mA are sinked continuously to maintain the gate discharged.

In order to withstand high dV/dt spikes a low resistive path between gate and source is implemented during the off state.

Figure 3:



DEVICE DESCRIPTION

Driver Supply

The High Side(HS) Driver is supplied from the internal charge pump buffered at CP_OUT.

The low-drop regulator provides approx. 4mA (f_{PWM} = 50KHz) per HS gate. In case of the full bridge that means approximately 16mA, 8.0 mA for the high side and 8.0 mA for the low side.

(Note: The average current required to switch a gate with a frequency of 100KHz is:

Average Current (Charge Pump) for PWM Frq. (f_{PWM})

$I_{CP} = Q_g * f_{PWM} = 80nC * 100\ kHz = 8.0mA$

A full bridge application switch only one high side and one low side at the same time.)

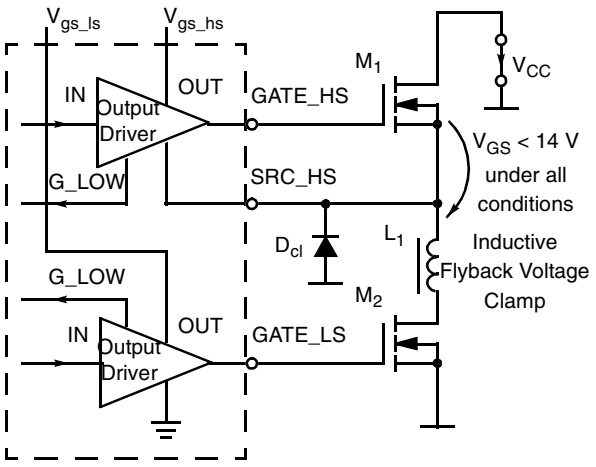
External capacitors on Charge Pump and on Linear Regulator are necessary to supply high peak current absorbed during switching. The Low Side Driver is supplied from built in low drop regulator.

Gate Protection

The low side gate is protected by the internal linear regulator, which guarantees that V_{GATE_LS} does not exceed the maximum V_{GS}. Especially when working with the charge pump the voltage at POS_HS can be up to 65V. The high side gate is clamped internally, in order to avoid a V_{GS} exceeding 18V.

The Gate protection does not include a Flyback Voltage Clamp that protects the driver and the external FET from a Flyback voltage that can appear when driving inductive load.This Flyback voltage can reach high negative voltage values and needs to be clamped externally.

Figure 4: Gate Protection & Flyback Voltage Clamp



TMOS Failure Protection

All output driver stages are protected against TMOS failure conditions. If one of the external power FETs is destroyed (Gate = V_{CC}, or Gate = Gnd) the function of the remaining output driver stages is not affected. All output drivers are short circuit protected against short circuits to ground.

Logic Inputs

Logic Input Voltage Range:

Absolute Max :

-0.3V ... 10V

Wake Up Function: (G_EN)

4.5V ... V_{CC2}

During Wake-Up the logic is supplied from the G_EN pin.

Low Drop Linear Regulator

The low drop linear regulator provides the 5.0V for the logic section of the driver, the V_{gs_ls} buffered at LR_OUT and the +14.5V for the charge pump, which generates the V_{gs_hs}.

The low drop linear regulator provides 4.0mA average current per driver stage. If typically V_{CC2} exceeds 15.0V the output is limited to $14.5V_{typ}$.

Charge Pump

The charge pump generates the high side driver supply voltage (V_{GS_HS}), buffered at CP_OUT.

$V_{gs\_hs} = V_{CC} + V_{LR\_OUT} - 2V$.

The average output current is I_{CP} = 4.0 mA (f_{PWM} = 50 KHz) per output driver.

The charge pump charges an external storage capacitor, which provides the peak switching current to the high side output drivers.

N.B. In some applications a large dV/dt at Pin C2 due to sudden changes at V_{CC} can cause a large peak currents flowing through Pin C1.

Positive transitions at Pin C2 ;mimimum peak current :

$I_{c1}min = 2.0A$

$t_{c1}min = 600ns$ (see Figure 5:for peak description)

Negative transitions at Pin C2; maximum peak current :

$I_{c1}max = 2.0A$

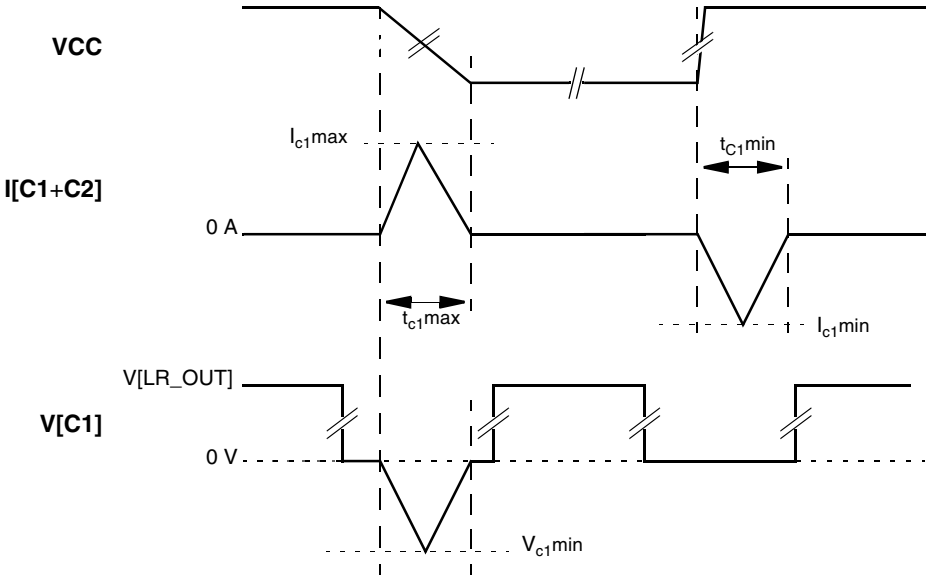
$t_{c1}max = 600ns$ (see Figure 5 for peak description)

Current sourced by Pin C1 during a large dV/dt will result in a negative voltage at Pin 13; negative transitions at Pin C2; minimum peak voltage:

$V_{c1}min = -1.5V$

$t_{c1}max = 600ns$ (see Figure 5:for peak description)

Figure 5: Limits of C1 Current & Voltage with Large Values dV/dt of Vcc



Over / Under Voltage Shutdown

The under voltage protection becomes active at V_{CC} below 5.5 V and the overvoltage protection is activated at V_{CC} above 55 V or at V_{CC2} above 28 V.

If the O/UV protection is activated the outputs are driven low, in order to switch off the FETs.

Protection

A protection against double battery and load dump spikes up to 55 V is given by V_{CC} = 55 V.

A protection against reverse polarity is given by the external power FET with the free wheeling diodes, forming a conducting pass from ground to V_{CC}. An additional protection is not provided within the circuit.

There is a temperature shut down protection per each half bridge. It protects the circuitry against temperature damage by blocking the output drives.

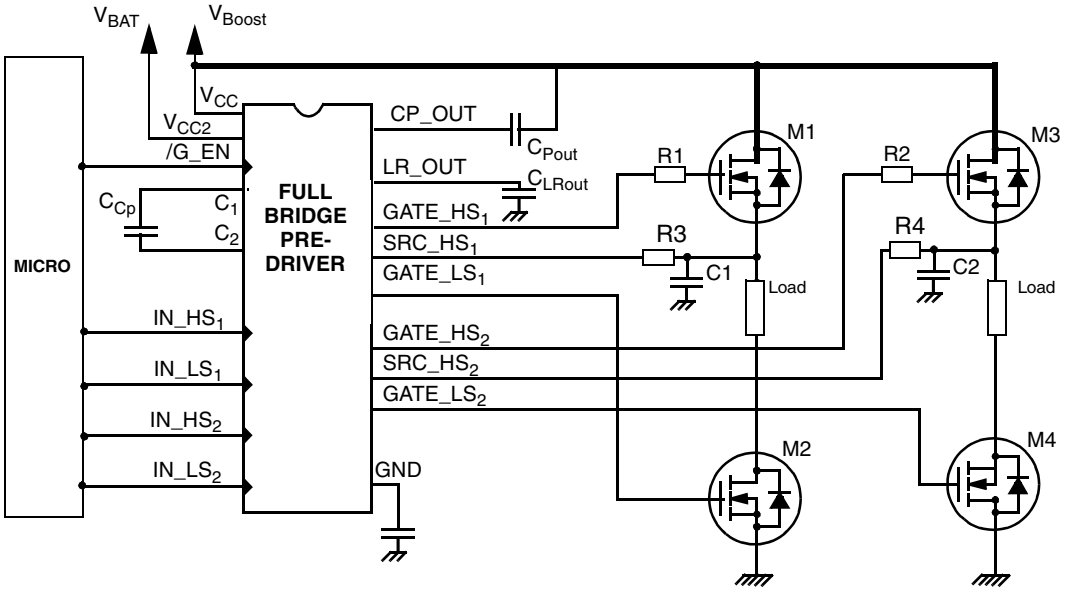
Both applications use the internal charge pump to provide the high side floating voltage. This voltage can be provided by an external source also.

The following figure shows a typical application.

It is worth noting that the supplies VBAT and Vboost may be independant , with different voltage values.

In the case of rapidly changing Vboost voltages, the large dv/dt may result in perturbations of the High Side driver such that the driver is forced into an OFF state. The addition of capaitors C1 & C2 reduces the dv/dt of the source line, consequently reducing driver perturbation.

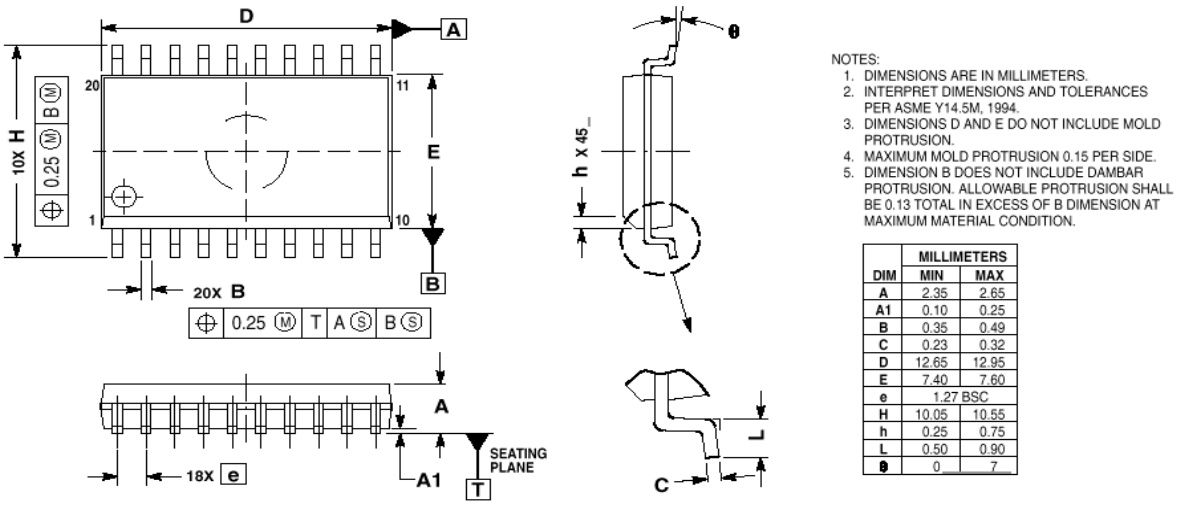
Figure 6: Block Diagram



PIN FUNCTION DESCRIPTION

Pin	Symbol	Pin Description
1	V_{CC}	Supply 1
2	C2	Charge Pump Capacitor
3	CP_OUT	Charge Pump Out
4	SRC_HS1	Source 1 Output High Side
5	GATE_HS1	Gate 1 Output High Side
6	IN_HS1	Pos. Input High Side 1
7	IN_LS1	Pos. Input High Side 1
8	GATE_LS1	Gate 1 Output Low Side
9	GND1	Ground
10	LR_OUT	Linear Regulator Output
11	V_{CC2}	Supply 2
12	GND_A	Analog Ground
13	C1	Charge Pump Capacitor
14	GND2	Ground 2
15	GATE_LS2	Gate 2 Output Low Side
16	IN_LS2	Pos. Input Low Side 2
17	IN_HS2	Pos. Input High Side 2
18	GATE_HS2	Gate 2 Output High Side
19	SRC_HS2	Source 2 Output High Side
20	G_EN	Global Enable

Package Description



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

CASE 751D–05
ISSUE F

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